Exploring the Impact of Domain Numbers on Negative Capacitance Effects in Ferroelectric Device-Circuit Co-Design

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Abstract—This paper explores the performance of HZO-stacked negative gate capacitance field-effect transistor (NCFET) for beyond CMOS technology. For the first time, we investigate the impact of ferroelectric (FE) domain numbers ($D_N$) on the NC effect, energy dissipation, polarization ramping rate, voltage amplification ($A_{NC}$), and operating frequency ($f_{osc}$) of the NCFET-ring oscillator (RO). The results show that HZO-NCFET is suitable for low-voltage and high-speed applications, providing a significant increase in $A_{NC}$ concerning the conventional PZT-NCFET and (P)VDF-TrFe)-NCFET. Finally, the proposed HZO-NCFET-RO shows superior performance with a 26% higher $f_{osc}$ and a 94.42% reduction in power dissipation compared to standard CMOS FET-RO. These findings highlight the potential of HZO-stacked NCFET as an alternative for the future beyond CMOS technology.

Keywords—Beyond CMOS; ferroelectric; hafnia; negative capacitance; ring oscillator; TCAD.

I. INTRODUCTION

The discovery of ferroelectricity and the NC effect in doped HfO$_2$ has sparked significant research interest in HZO-based FETs. This is because of their capability to overcome Boltzmann’s Tyranny, a substantial limitation of traditional CMOS FETs [1], [2]. Thin film HZO have been extensively investigated due to their compatibility with CMOS and sub-10 nm scalability. They have been researched for potential integration into nanoscale devices, including nonvolatile memories, FE tunnel junctions, and NCFETs. These devices are designed to address energy issues in VLSI and enable ultralow power applications [1]–[9]. However, the impact of thin-film HZO’s $D_N$ on the NC effect in NC-based device-circuit co-design issues is missing in the literature. The objective of this paper is to explore the influence of $D_N$ on several factors related to the TiN/HZO/TiN (MFM) stack, including the dynamic NC effect, QV response, charge, and current. We show that higher levels of $D_N$ lead to greater energy dissipation in the form of heat through $R$. We implemented HZO-NCFET and examined how $D_N$ affects $A_{NC}$ at low and high operating frequencies. We compared the performance of the HZO-NCFET with its counterpart, the PZT and (P)VDF-TrFe)-NCFET. Finally, we proposed a 5-stage NCFET-RO running at GHz speed and ultralow power compared to the state-of-the-art RO.

Fig. 1. (a) Schematic of an R-MFM stack. (b) Calibration of Landau’s $F_z$ anisotropy coefficients with experimental data [2]. (c) Schematic of HZO-NCFET and its equivalent circuit diagram. (d) Transfer curve calibration of 45 nm Intel CMOS FET with experimental data [3].

II. MODELING AND SIMULATION

The investigated MFM stack features a 7.7 nm thin HZO film with 12 nm TiN electrodes on top and bottom. TiN electrodes were used due to HZO’s favorable FE properties between them. The TCAD [4] simulation setup includes $R$ and MFM stack in series [Fig. 1(a)], along with a gate input signal, $V_G$ drifting from $-2.5$ to $+2.5$ V. A library for HZO is added to the default simulation setup, incorporating its bandgap (5.9 eV), relative permittivity (25), electron affinity (2.05 eV), and polarization ($P$) properties. The TCAD tools read and process the HZO library, precisely considering the physical and electrical properties of every material utilized in the analysis. The NC effect in HZO can be modeled using the Ginzburg-Landau-Khalatnikov (GLK) model [4]. The equation governing the evolution of $P$ can be derived from the gradient flow of the free energy ($F_0$).

$$
\xi (\xi (dP/dt) + \xi F_0) = 0
$$

$$
V_{FE}\left(\frac{2aP + 4bP^2}{6yP}\right) + \xi F_0 = 0
$$

For HZO, $\xi = 0.18$ Gcm from optical measurement [5], $g = 1 \times 10^{-3}$ cm$^3$/F [6] represents $D_N$ coupling coefficients. Finally, the Landau coefficients ($\alpha = -1 \times 10^{11}$ cm/F, $\beta = 2.5 \times 10^{20}$ cm$^3$/F$^2$), $\gamma = 0$ are extracted from the measured $PE$ curve [2], as shown in Fig. 1(b). Finally, the HZO-NCFET is modeled by integrating the GLK-based MFM stack on top of the experimentally validated 45 nm Intel CMOS FET [3], [7], as shown in Fig. 1(c–d).
It’s crucial to study the switching behavior of the MFM stacked NCFET to assess its potential for designing high-speed and low-voltage digital circuits. In Fig. 3(a-b), the proposed HZO-NCFET maintains an $A_{SC}$ of 1.65 V at low and high frequencies, while the PZT-NCFET can only provide 1.4 V at low frequencies and fails to provide any $A_{SC}$ at high frequencies meaning that HZO-NCFET is suitable for high-speed and low-voltage applications. In Fig. 3(c), $A_{SC}$ exponentially decreases as $D_N$ increases at low and high frequencies. This is because when $D_N$ increases, a larger number of domains interact with each other, leading to a decrease in $P$ switching and the NC effect. HZO-NCFET provides a 17.86% and 13.79% increase in $A_{SC}$ compared to PZT-NCFET [8] and P(VDF-TrFE)-NCFET [9], respectively, as shown in Fig. 3(d).

The HZO-NCFET-RO in Fig. 4(a) is essential for advancing beyond CMOS technologies. It allows for easy evaluation of NCFET performance and guides design and technology co-optimization. By measuring the RO’s propagation delay time ($\tau$), critical parameters like $f_{OSC}$ and power dissipation ($P_{DC}$) can be estimated and compared to other technologies. We implemented a 5-stage RO using the proposed HZO-NCFET-based inverters and juxtaposed its performance with the conventional CMOS FET-RO, as shown in Fig. 4(b). In terms of speed, the 5-stage RO implemented using HZO-NCFET-based inverters have a lower $\tau$, 47.55% lower than the conventional CMOS FET-RO due to the higher on-current of HZO-NCFET-based inverters. In Fig. 4(c), we note that $f_{OSC}$ decreases almost linearly as $D_N$ increases. This is because $P$ switching slacks off at larger $D_N$, causing higher $\tau$ values, resulting in lower $f_{OSC}$. Finally, Fig. 4(d) compares the proposed 5-stage HZO-NCFET-RO with an industry-standard 5-stage CMOS-RO [10]. Compared to the CMOS-RO [10], HZO-NCFET-RO achieved a 26% increase in $f_{OSC}$ and a 94.42% decrease in $P_{DC}$.

IV. CONCLUSION

The study provides critical insights into the impact of the number of domains on the performance of MFM-stacked NCFETs and highlights the potential of HZO-NCFET for high-speed and low-voltage applications. The proposed HZO-NCFET-RO could be essential for advancing beyond CMOS technologies, and the findings could guide design and technology co-optimization.

REFERENCES